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EXAMINER	
DHARIA, PRABODH M	

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11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/850,053	Applicant(s) INUKAI, KAZUTAKA	
	Examiner Prabodh M Dharia	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-49 and 132-165* is/are pending in the application.

4a) Of the above claim(s) *50-63* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36,37,39-49,132,133,135-145,147-157 and 159-165* is/are rejected.

7)☐ Claim(s) *38,134,146 and 158* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. **Status:** Receipt is acknowledged of papers submitted on 05-19-2004 under request for reconsideration has been placed of record in the file. Claims 36-49,132-167 are pending in this action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. Claims 36,37,39-49,132,133,135-145,147,157 and 159-167 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (6,635,505 B2).

Regarding Claim 36, Tanaka et al. teaches a light emitting device (EL display, LCD display) (Col. 27, Line 15, Col. 5, Lines 53-55) comprising: a source signal line driver circuit (Col. 3, Lines 40-43); a gate signal line driver circuit (Col. 3, Lines 43-45); an opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); a pixel portion

comprising a plurality of pixels (Col. 5, Lines 58-60); a plurality of source signal lines connected to the source signal line driver circuit (Col. 3, Lines 21-24); a plurality of gate signal lines connected to the gate signal line driver circuit (Col. 3, Lines 23-25); a plurality of opposing power source lines connected to the opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); and a plurality of power source supply lines (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4), wherein each pixel comprises: a switching TFT (Col. 3, Lines 25,26) having a gate electrode connected to any one of the plural gate signal lines (Col. 3, Lines 29,30) and a source region and a drain region, one of which is connected to any one of the plural source signal lines (Col. 3, Lines 23-30, figure 30B, Col. 32, Lines 45-59, Col. 20, Lines); an electro luminescence driver TFT, a gate electrode of said electro luminescence driver TFT connected to the other of said source region and said drain region of switching TFT (figure 30B, Col. 32, Lines 45-59, Col. 24, Lines 4-17, Col. 23, Lines 45,46, Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46); an electro luminescence element comprises a pixel electrode, an opposing electrode connected to any one of the plural opposing power source lines (figure 30B, Col. 32, Lines 45-59)., and an electro luminescence layer provided between the pixel electrode and the opposing electrode; wherein the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines (figure 30B, Col. 32, Lines 45-59) and the electro luminescence driver TFT has a drain region connected to the pixel electrode (figure 30B, Col. 32, Lines 45-59).

Regarding Claim 37, Tanaka et al. teaches the electro luminescence layer is formed of a monomer organic material or a polymer organic material (Col. 31, Lines 3-7).

Regarding Claim 39, Tanaka et al. teaches the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate (Col. 31, Lines 3-7).

Regarding Claim 40, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58); it is obvious to one in the ordinary skill in the art when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

Regarding Claim 41, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58).

Regarding Claim 42, Tanaka et al. teaches the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring (Col. 27, lines 12-43, Col. 28, Lines 5-27, Lines 62-67)

Regarding Claim 43, Tanaka et al. teaches the bank has a light-shielding property (Col. 22, Lines 39-43).

Regarding Claim 44, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of top gate type (Col. 23, Lines 14-17).

Regarding Claim 45, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of bottom gate type (Col. 23, Lines 14-17).

Regarding Claim 46, Tanaka et al. teaches the electro luminescence driver TFT is driven in a linear range (Col. 30, Lines 9-13 since switching TFT operates in Linear region as they saturate and active region turned on and turned off, Col. 24, Lines 31-36)

Regarding Claim 47, Tanaka et al. teaches the light emitting device is a computer (Col. 25, Lines 5-15).

Regarding Claim 48, Tanaka et al. teaches the light emitting device is a video camera (Col. 25, Lines 5-15).

Regarding Claim 49, Tanaka et al. teaches the light emitting device is a DVD player (Since computer or TV player uses recording medium and display information of DVD this invention is applicable to the display device; Col. 25, Lines 5-15).

Regarding Claim 132, Tanaka et al. teaches a light emitting device (EL display, LCD display) (Col. 27, Line 15, Col. 5, Lines 53-55) comprising: a source signal line driver circuit

(Col. 3, Lines 40-43); a gate signal line driver circuit (Col. 3, Lines 43-45); an opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); a pixel portion comprising a plurality of pixels (Col. 5, Lines 58-60); a plurality of source signal lines connected to the source signal line driver circuit (Col. 3, Lines 21-24); a plurality of gate signal lines connected to the gate signal line driver circuit (Col. 3, Lines 23-25); a plurality of opposing power source lines connected to the opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); and a plurality of power source supply lines (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4), wherein each pixel comprises: a switching TFT (Col. 3, Lines 25,26) having a gate electrode connected to any one of the plural gate signal lines (Col. 3, Lines 29,30) and a source region and a drain region, one of which is connected to any one of the plural source signal lines (Col. 3, Lines 23-30, figure 30B, Col. 32, Lines 45-59, Col. 20, Lines); an electro luminescence driver TFT, a gate electrode of said electro luminescence driver TFT connected to the other of said source region and said drain region of switching TFT (figure 30B, Col. 32, Lines 45-59).; an electro luminescence element comprises a pixel electrode, an opposing electrode connected to any one of the plural opposing power source lines (figure 30B, Col. 32, Lines 45-59, figure 30B, Col. 32, Lines 45-59, Col. 24, Lines 4-17, Col. 23, Lines 45,46, Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46)., and an electro luminescence layer provided between the pixel electrode and the opposing electrode; wherein the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines (figure 30B, Col. 32, Lines 45-59) and the electro luminescence driver TFT has a drain region connected to the pixel electrode (figure 30B, Col. 32, Lines 45-59).

Regarding Claim 133, Tanaka et al. teaches the electro luminescence layer is formed of a monomer organic material or a polymer organic material (Col. 31, Lines 3-7).

Regarding Claim 135, Tanaka et al. teaches the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate (Col. 31, Lines 3-7).

Regarding Claim 136, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58); it is obvious to one in the ordinary skill in the art when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

Regarding Claim 137, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58).

Regarding Claim 138, Tanaka et al. teaches the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring (Col. 27, lines 12-43, Col. 28, Lines 5-27, Lines 62-67)

Regarding Claim 139, Tanaka et al. teaches the bank has a light-shielding property (Col. 22, Lines 39-43).

Regarding Claim 140, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of top gate type (Col. 23, Lines 14-17).

Regarding Claim 141, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of bottom gate type (Col. 23, Lines 14-17).

Regarding Claim 142, Tanaka et al. teaches the electro luminescence driver TFT is driven in a linear range (Col. 30, Lines 9-13 since switching TFT operates in Linear region as they saturate and active region turned on and turned off, Col. 24, Lines 31-36).

Regarding Claim 143, Tanaka et al. teaches the opposing power source lines are arranged such that adjacent pixels that are connected to a common source signal lines are connected to different opposing power source (Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46).

Regarding Claim 144, Tanaka et al. teaches a personal computer (Col. 1, Lines 23-26, Col. 25, Lines 20-23) comprising a EL display with a main body (Col. 25, Lines 20-23, Col. 30, Lines 15-17, Col. 29, Line 56) and a keyboard (Col. 1, Lines 23-26, Col. 25, Lines 20-23, it is well known to one ordinary skill in the art, the note book computer Tanaka et al. teaches has

built in keyboard) with EL display device (Col. 27, Line 15, Col. 5, Lines 53-55) comprising: a source signal line driver circuit (Col. 3, Lines 40-43); a gate signal line driver circuit (Col. 3, Lines 43-45); an opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); a pixel portion comprising a plurality of pixels (Col. 5, Lines 58-60); a plurality of source signal lines connected to the source signal line driver circuit (Col. 3, Lines 21-24); a plurality of gate signal lines connected to the gate signal line driver circuit (Col. 3, Lines 23-25); a plurality of opposing power source lines connected to the opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); and a plurality of power source supply lines (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4), wherein each pixel comprises: a switching TFT (Col. 3, Lines 25,26) having a gate electrode connected to any one of the plural gate signal lines (Col. 3, Lines 29,30) and a source region and a drain region, one of which is connected to any one of the plural source signal lines (Col. 3, Lines 23-30, figure 30B, Col. 32, Lines 45-59, Col. 20, Lines); an electro luminescence driver TFT, a gate electrode of said electro luminescence driver TFT connected to the other of said source region and said drain region of switching TFT (figure 30B, Col. 32, Lines 45-59).; an electro luminescence element comprises a pixel electrode, an opposing electrode connected to any one of the plural opposing power source lines (figure 30B, Col. 32, Lines 45-59, figure 30B, Col. 32, Lines 45-59, Col. 24, Lines 4-17, Col. 23, Lines 45,46, Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46)., and an electro luminescence layer provided between the pixel electrode and the opposing electrode; wherein the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines (figure 30B, Col. 32, Lines 45-59) and the

electro luminescence driver TFT has a drain region connected to the pixel electrode (figure 30B, Col. 32, Lines 45-59).

Regarding Claim 145, Tanaka et al. teaches the electro luminescence layer is formed of a monomer organic material or a polymer organic material (Col. 31, Lines 3-7).

Regarding Claim 147, Tanaka et al. teaches the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate (Col. 31, Lines 3-7).

Regarding Claim 148, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58); it is obvious to one in the ordinary skill in the art when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

Regarding Claim 149, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58).

Regarding Claim 150, Tanaka et al. teaches the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and wherein a bank is formed on a region where the pixel electrode is connected to the drain region

of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring (Col. 27, lines 12-43, Col. 28, Lines 5-27, Lines 62-67)

Regarding Claim 151, Tanaka et al. teaches the bank has a light-shielding property (Col. 22, Lines 39-43).

Regarding Claim 152, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of top gate type (Col. 23, Lines 14-17).

Regarding Claim 153, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of bottom gate type (Col. 23, Lines 14-17).

Regarding Claim 154, Tanaka et al. teaches the electro luminescence driver TFT is driven in a linear range (Col. 30, Lines 9-13 since switching TFT operates in Linear region as they saturate and active region turned on and turned off, Col. 24, Lines 31-36).

Regarding Claim 155, Tanaka et al. teaches the opposing power source lines are arranged such that adjacent pixels that are connected to a common source signal lines are connected to different opposing power source (Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46).

Regarding Claim 156 Tanaka et al. teaches A cellular telephone comprising a main body, an audio output portion, an audio input portion, (Col. 25, Lines 12-15) with the display portion (EL display, LCD display) (Col. 27, Line 15, Col. 5, Lines 53-55) comprising: a source signal line driver circuit (Col. 3, Lines 40-43); a gate signal line driver circuit (Col. 3, Lines 43-45); an opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); a pixel portion comprising a plurality of pixels (Col. 5, Lines 58-60); a plurality of source signal lines connected to the source signal line driver circuit (Col. 3, Lines 21-24); a plurality of gate signal lines connected to the gate signal line driver circuit (Col. 3, Lines 23-25); a plurality of opposing power source lines connected to the opposing power source line driver circuit (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4); and a plurality of power source supply lines (Col. 3, Lines 55-58, Col. 2, Line 65 to Col. 3, Line 4), wherein each pixel comprises: a switching TFT (Col. 3, Lines 25,26) having a gate electrode connected to any one of the plural gate signal lines (Col. 3, Lines 29,30) and a source region and a drain region, one of which is connected to any one of the plural source signal lines (Col. 3, Lines 23-30, figure 30B, Col. 32, Lines 45-59, Col. 20, Lines); an electro luminescence driver TFT, a gate electrode of said electro luminescence driver TFT connected to the other of said source region and said drain region of switching TFT (figure 30B, Col. 32, Lines 45-59).; an electro luminescence element comprises a pixel electrode, an opposing electrode connected to any one of the plural opposing power source lines (figure 30B, Col. 32, Lines 45-59, figure 30B, Col. 32, Lines 45-59, Col. 24, Lines 4-17, Col. 23, Lines 45,46, Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46), and an electro luminescence layer provided between the pixel electrode and the opposing electrode; wherein the electro luminescence driver TFT has a source region connected to any one of the plural power

source supply lines (figure 30B, Col. 32, Lines 45-59) and the electro luminescence driver TFT has a drain region connected to the pixel electrode (figure 30B, Col. 32, Lines 45-59).

Regarding Claim 157, Tanaka et al. teaches the electro luminescence layer is formed of a monomer organic material or a polymer organic material (Col. 31, Lines 3-7).

Regarding Claim 159, Tanaka et al. teaches the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate (Col. 31, Lines 3-7).

Regarding Claim 160, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58); it is obvious to one in the ordinary skill in the art when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

Regarding Claim 161, Tanaka et al. teaches when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT (Col. 28, Lines 15-26, Col. 30, Line 8, Lines 55-58).

Regarding Claim 162, Tanaka et al. teaches the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and wherein a bank is formed on a region where the pixel electrode is connected to the drain region

of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring (Col. 27, lines 12-43, Col. 28, Lines 5-27, Lines 62-67).

Regarding Claim 163, Tanaka et al. teaches the bank has a light-shielding property (Col. 22, Lines 39-43).

Regarding Claim 164, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of top gate type (Col. 23, Lines 14-17).

Regarding Claim 165, Tanaka et al. teaches the switching TFT or the electro luminescence driver TFT is of bottom gate type (Col. 23, Lines 14-17).

Regarding Claim 166, Tanaka et al. teaches the electro luminescence driver TFT is driven in a linear range (Col. 30, Lines 9-13 since switching TFT operates in Linear region as they saturate and active region turned on and turned off, Col. 24, Lines 31-36).

Regarding Claim 167, Tanaka et al. teaches the opposing power source lines are arranged such that adjacent pixels that are connected to a common source signal lines are connected to different opposing power source (Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46).

Allowable Subject Matter

4. Claims 38,134,146,158 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance: The cited refrence of Tanaka et al. (6,635,505 B2) fails to teach the monomer organic material comprises Alq_3, (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments filed 05-19-2004 have been fully considered but they are not persuasive.

Applicant argues the cited reference of Tanaka et al. fails to teach opposing power source line.

Examiner disagrees as Tanaka et al. does teach opposing power source line (figure 30B, Col. 32, Lines 45-59, figure 30B, Col. 32, Lines 45-59, Col. 24, Lines 4-17, Col. 23, Lines 45,46, Col. 8, Line 48 to Col. 9, Line 5, Col. 3, Lines 35-38, Col. 2, Lines 39-46).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2673

06-17-2004

VIJAY SHANKAR
PRIMARY EXAMINER